

# Multi-tier die stacking through collective die-to-wafer hybrid bonding.

Koen Kennes<sup>1\*</sup>, Ye Lin<sup>1</sup>, Samuel Suhard<sup>1</sup>, Pieter Bex<sup>1</sup>, Dieter H. Cuyper<sup>1</sup>, Alice Guerrero<sup>2</sup>, Dennis Bumüller<sup>3</sup>, Alain Phommahaxay<sup>1</sup>, Gerald Beyer<sup>1</sup> and Eric Beyne<sup>1</sup>

<sup>1</sup>imec, Kapeldreef 75, 3001 Leuven, Belgium

<sup>2</sup>Brewer Science, Inc., 2401 Brewer Drive, Rolla, MO 65401, USA

<sup>3</sup>SUSS MicroTec Lithography GmbH, Ferdinand-von-Steinbeis-Ring 10, 75447 Sternefeld, Germany

\*Phone: +32-16-28-79-05

E-mail: koen.kennes@imec.be

**Abstract**—A collective die-to-wafer bonding flow is extended beyond the N=2 tier to the N=3 and N=4 tier by collectively bonding multiple layers of dies on top of a target wafer. The N=2 die-level is shown to be consistently free of bonding voids (bond yields close to 100%) with +99% die transfer yields. For the N=3 and N=4 die-levels, both the transfer yields and bonding yields are significantly lower. Both N=2 and N=3 stacks show similar die-to-target wafer alignment. A cross sectional SEM of a 5-micron pitch shows excellent alignment and connectivity between Die 1 and Die 2 (N=3).

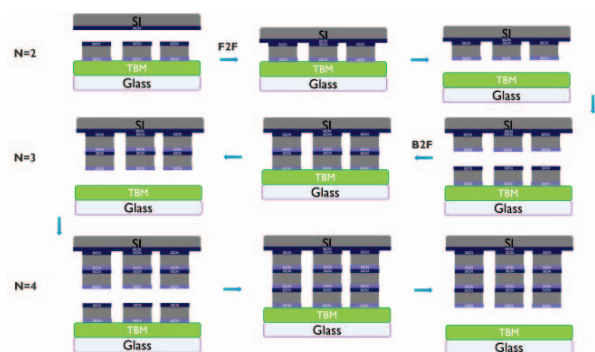
**Keywords**—Heterogeneous integration, wafer bonder, dielectric bonding, hybrid bonding, die-to-wafer bonding, temporary bonding material, laser release material, laser debonding, collective hybrid bonding, die stacking

## I. INTRODUCTION

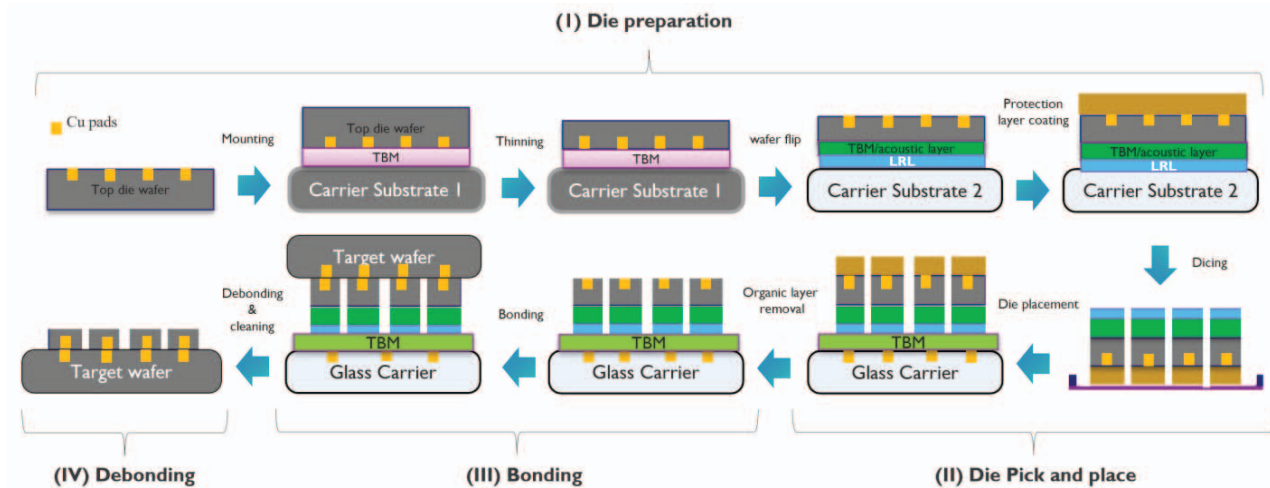
Certain 3D IC technologies require a vertical interconnect with high connectivity densities between dies. [1-3] A high alignment accuracy follows and as such the choice of process favors a hybrid bonding process. Both collective die-to-wafer bonding and direct die-to-wafer bonding schemes are attractive in this regard. [4-6] Where a direct bonding flow seems much less complex compared to a collective bonding flow, there remain limitations regarding die-level cleanliness. Much progress has been made though, by enabling a wafer level cleaning approach before die pick up. However, during the final pick-up step the sensitive bond surface will be in contact with the die-placement tool leading to very stringent tool-cleanliness requirements or in situ die-level cleaning capability. In contrast, a collective die-to-wafer bonding flow, although more complex, allows all processing on wafer-level tools and as such allows inspection of the die level bonding surface prior to bonding. In several previous reports [5-10], imec's proposed flows were explained in detail. It was shown that very thin dies (50  $\mu\text{m}$ ) or thick dies (775  $\mu\text{m}$ ) can be transferred from a temporary carrier to a target wafer with transfer yields and bond yields close to

100%. Several flavors of the collective die-to-wafer flow exist within imec. The choice of temporary carrier system will depend strongly on the die type. For ultra-thin and flat dies (50  $\mu\text{m}$ ) a silicon carrier system can be used that allows mechanical debonding of the dies with transfer yields up to unity. [9, 10] Mechanical debonding has the advantage of using silicon carriers. On the other hand, using glass offers the benefit of UV-laser debonding. [5, 7, 9]

Whenever dies become either too thick, too warped or simply have a different backside, the final touch to the adhesive of the carrier system might be impacted. Finetuning adhesion to enable wafer level cleaning (without losing dies) and still allowing a mechanical peel debond often results in either a limited die transfer or extensive die damage. [7] Solving die-temporary carrier adhesion issues can be time consuming and very die-dependent. As such a glass carrier was introduced for



**Figure 1. Simplified flow for N=2, N=3 and N=4 collective die-to-wafer transfer.**



**Figure 2. The collective-hybrid die-to-wafer bonding flow. After thinning on a temporary carrier, the laser release layer (blue layer) and acoustic layer (green) are introduced during the wafer flip to enable the coating of the protection layer (orange). After flipping the thin wafer on tape frame, the stack is singulated. Dies are picked up and place on a final temporary carrier where the dies are cleaned, bonded and debonded.**

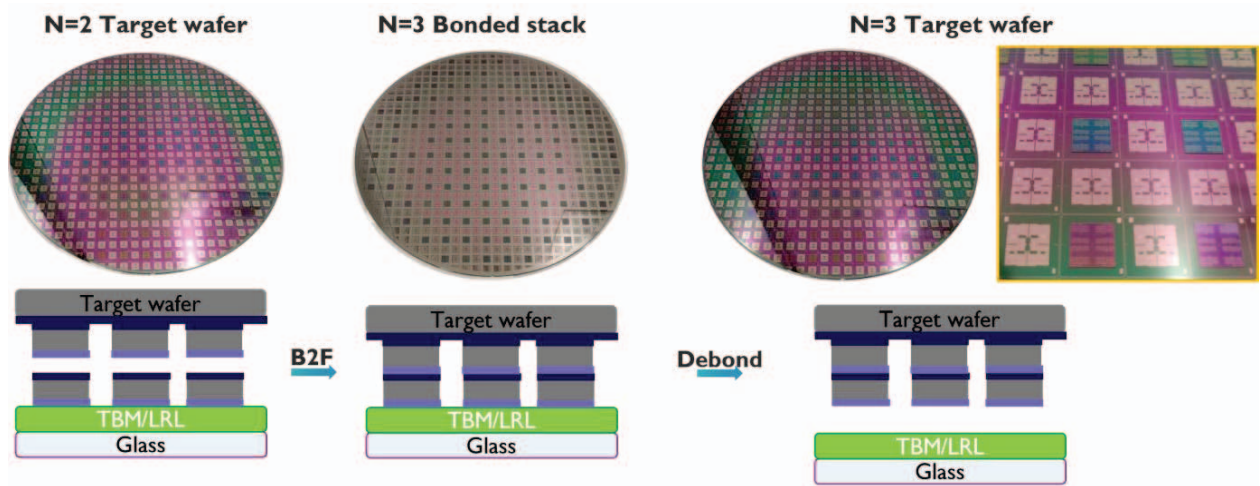
the final debonding step together with a laser release layer (LRL) on the dies [5, 9]. Although 100% die transfer could easily be achieved, 1-4% of the dies showed some damage during the process. A study was performed to assess potential laser damage to ultrathin dies. The main finding was that during the ablation process a shockwave is generated in the LRL that propagates to the thin die and leads to some damage at the corners of the dies. This damage can easily be avoided by separating the ablation interface from the die interface by either using a thick LRL or an additional temporary bond material (TBM) between the LRL and the die, (which we will call acoustic layer (AL). Using the latter methodology, 100% die transfer could be achieved with electrically yielding daisy chains and kelvin structures up to 80% for the 7- $\mu\text{m}$  pitch range [5].

The robustness of this flow was demonstrated several times for the  $N=2$  level, with  $N$  equal to the number of interfaces. Provided that the right dielectrics are present on the die backside, after die transfer the dies can be collectively cleaned and a second layer of dies can be bonded on top (Fig. 1). This step can be repeated  $X$  times to allow multi die stacking. In this publication the process of reference (POR) flow, using laser debonding and acoustic layer, is utilized to enable  $N=3$  and  $N=4$  stacks. As such a first layer of dies is transferred to the target wafer (tier 1) to enable  $N=2$ . During Tier 2 a second layer of dies is transferred on top of the first layer of dies to enable  $N=3$  and finally Tier 3 to enable  $N=4$ . Both non-aligned bonding and aligned bonds are shown. Finally, an  $N=3$  stack is prepared using electrically yielding dies in order to evaluate the connectivity between die 1 and die 2 using a cross sectional SEM of a 5-micron pitch connection.

## II. $N=3$ STACKS

The collective die-to-wafer flow consists of several parts: i) die preparation, ii) die pick and place, iii) bonding and iv) debonding. For the die preparation step, the wafer is flipped and mounted/bonded upside down to a temporary carrier using a temporary bonding system. The wafer is thinned down to 50  $\mu\text{m}$ , and the backside surface is prepared. For the short loop experiments the temporary bond system was BrewerBOND<sup>®</sup> 305 paired with BrewerBOND<sup>®</sup> 510 material which allows for an easy mechanical release during the subsequent wafer flip step. A low temperature SiCN is deposited as backside bonding dielectric. For the full loop dies, presented in section IV, Brewer's Versa layer system consisting of BrewerBOND<sup>®</sup> C1301 and BrewerBOND<sup>®</sup> T1107 was used. This system enables elevated temperature processing and much better CMP control during the preparation of the hybrid bond pads after TSV reveal. The details of the full loop die processing and results will be published elsewhere. After backside preparation the thin wafer is flipped again, this time to a glass carrier, and the frontside is thoroughly cleaned after which a photoresist is coated to protect the frontside dielectric. This wafer flip step and resist coating step has several functions: the resist protects the die-frontside from the tape used during dicing as well as from the dicing itself. The temporary bonding adhesive and laser release layer allow for a final flip onto tape frame to enable dicing. Both of the materials will be diced and re-used during the final collective die transfer step.

After dicing the dies are placed on a temporary glass carrier coated with BrewerBOND<sup>®</sup> C1301-50 material. The photoresist is removed, revealing the die frontside dielectric. A wafer-to-wafer bonding step (XBS300 D2W collective bonder from SUSS MicroTec) is applied followed by a laser removal of the temporary carrier using the XBC300 Gen2 Laser Debonder from SUSS MicroTec. Finally, the laser release layer and acoustic layers are stripped to reveal the  $N=2$  stack. This flow is then repeated one more time using the  $N=2$  stack as target wafer

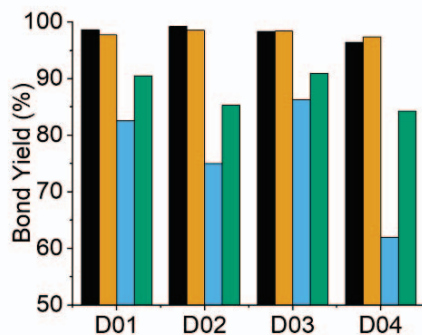


**Figure 3. Simplified collective die-to-wafer bonding flow with pictures of the N=2 target wafer (after tier 1), the N=3 bonded stack and the N=3 target wafer (after tier 2).**

leading to an N=3 stack and finally an N=4 stack. For all tier levels (tier 1-3) the same cleaning and bonding recipes were used with no special attention to optimization of individual recipes.

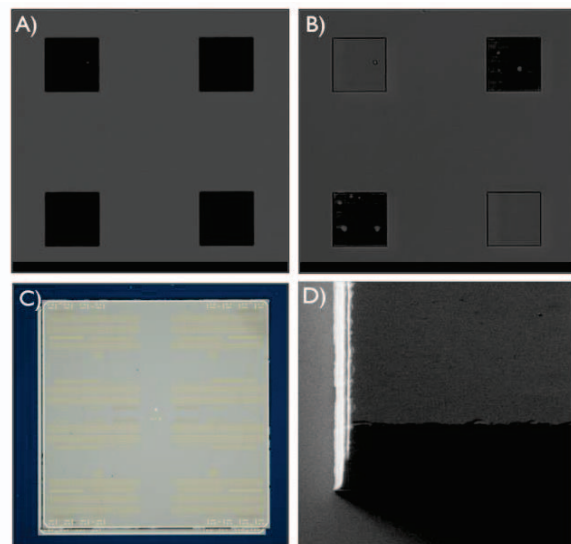
Four N=2 stacks were prepared and evaluated by calculating the transfer yields and bond yields. All prepared wafers had a transfer yield between 98-100% (Fig 3). The transfer yield is defined as the number of dies that were successfully transferred to the target wafer over the number of dies that were successfully populated on the temporary carrier. The bond yield (described in detail in [8]) is a measure of how void free the transferred dies are and are all close to 99%.

In the following step the four N=2 stacks were used to generate four N=3 stacks (Fig 3 & 4). In contrast to the Tier 1 transfers the transfer yields of Tier 2 vary strongly from stack to stack with the best result being 93% and the worst 64% (92%



**Figure 4. Bond yield for the N=2 interface after tier 1 (black), after tier 2 (orange) and bond yield of the N=3 interface (blue) and normalized over the number of transferred dies (green)**

and 84% for the two others). The lower transfer yields are also reflected in lower bond yields (Fig 4 & 6). The bond yields range between 60% and 85% however, this data is misleading due to the non-transferred dies. Normalizing the bond yield over the number of voids per transferred dies. These normalized bond yields range from 85 to 90%. This means that around 10-15% of the die area shows voiding indicative of a die-backside problem, caused either during back side processing or, more likely, an insufficient cleaning of the die backside after the Tier 1 transfer step. It is interesting to note that the bond yield of the Tier 1 layers (N=2) does not suffer from the Tier 2 step (Fig 4). Indeed,



**Figure 5. A) SAM of N=2 interface, B) SAM of the N=3 interface, C) optical image of 2 misaligned dies, D) SEM of 2 well aligned dies.**

extremely limited voiding can be seen for the Tier 1 interface

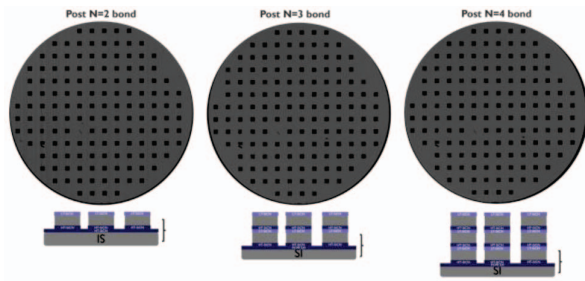


Figure 6. SAM images of the N=2 interface after tier 1, tier 2 and tier 3.

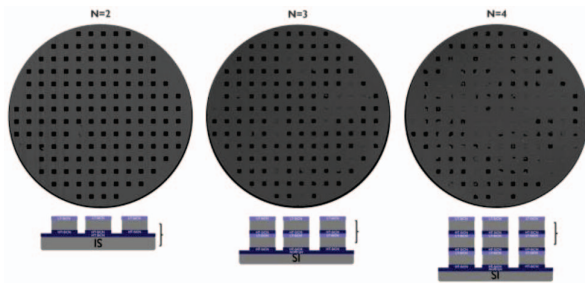


Figure 7. SAM images of the N=2 interface after tier 1, N=3 interface after tier 2 and N=4 interface after tier 3.

compared to the tier 2 interface (Fig 5 A&B). Due to the die thickness, after transfer of the second die-layer it is difficult to distinguish between a single die layer or a double die layer. The SAM measurement clearly reveals the missing dies (Fig 5B & 7). Further visualization of the double die stacks can be provided with IR microscopy (Fig 5C) and SEM imaging (Fig 5D).

The previous bonding steps were performed without any wafer-to-wafer alignment. In the next phase the alignment of the

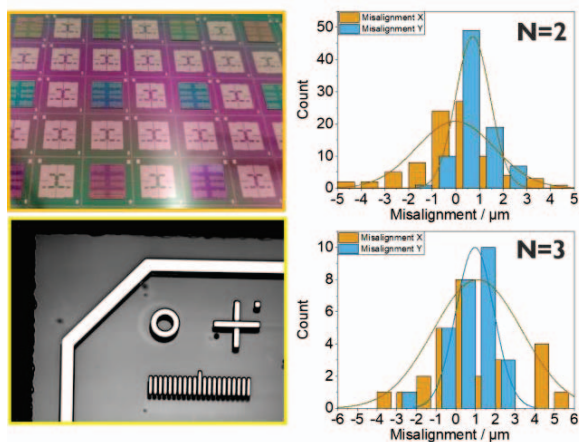


Figure 8. Picture of an N=3 stack (top left), IR image of the top corner of the stack (bottom left) and the die-to-target wafer alignment of the N=2 stack and N=3 stack.

dies with respect to the target wafer was investigated. An additional N=2 stack was prepared where the carrier wafer was aligned to the target wafer during the bonding process. After debonding an IR microscope was used to measure the alignment between the tier 1 dies with respect to the target wafer (Fig 8). The majority of the dies have an alignment better than  $\pm 2\mu\text{m}$ . Note that the die alignment is limited by the alignment precision of the die-placement tool ( $\sim 2\mu\text{m}$  (3s)) and wafer bonder tool ( $\sim 45\text{nm}$  (3s)) used. After the transfer of the tier 2 dies the die-to-target wafer alignment was measured. Also, for these dies the majority of the dies is below  $\pm 2\mu\text{m}$ . Unfortunately, due to the design of the alignment markers, it was not possible to measure all tier 2 dies nor the exact alignment between the tier 1 and tier 2 dies since their respective markers overlap (Fig 8).

### III. N=4 STACK

It is evident that more optimization is needed to increase both the die transfer yield as well as the bond yield for the N=3 stacks generated through this collective die-to-wafer transfer process. Such optimizations will need to include a proper inspection of the die-backsides after tier 1 transfer and likely several cleaning steps within this flow will require optimizations as well. Further improvements can only be made once die-level inspection methods are optimized. The optimizations considered here will be discussed in an upcoming publication dedicated to backside processing steps related to collective die to wafer hybrid bonding. Nevertheless, these N=3 results are considered promising and demonstrate the potential of this flow. The best N=3 stack was submitted to a final round of the collective die-to-wafer transfer process to enable an N=4 stack.

The Tier 3 (N=4) transfer process had an exceptionally low transfer yield (48%). Half of the dies were not transferred. For the N=3 process we could clearly distinguish the N=2 level from the N=3 level using scanning acoustic microscopy, however, although we can easily measure the N=2 level of this N=4 stack it turned out to be exceedingly difficult to distinguish between the N=3 and N=4 level (Fig 6 and 7). Hence, the die-transfer yield was assessed using IR microscopy (Fig 9).

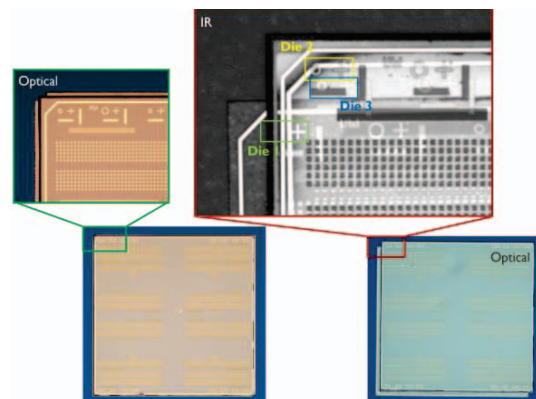
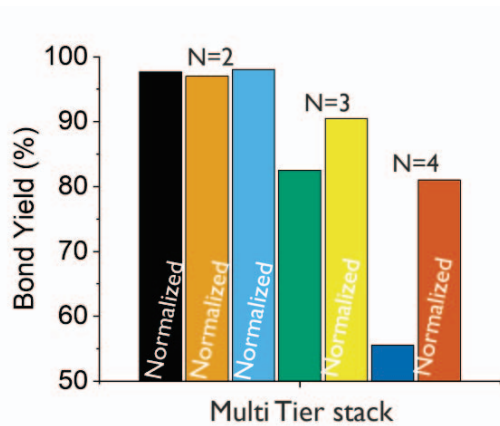


Figure 9. Optical and IR images of several N=4 stacks.

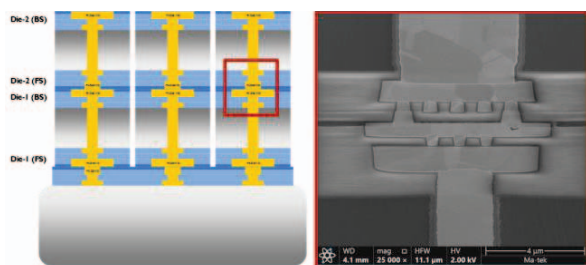


**Figure 10. Bond yields for the N=2, 3 and 4 stacks as calculated from Figures 6 and 7.**

Considering the fact that the bond yield as measured via SAM for the N=2 stack measured after every transfer process from N=2 to N=3 to N=4 is identical within the measurement limits (SAMs on Fig 6 and calculated values in Fig 10) it is reasonable to assume that the tier 3 has a similar low impact on tier 2. If this is true, then we can consider the measured SAM to be mostly stemming from the N=4 level (Fig 7). The calculated bond yield in this case is only 55% (Fig 10). Normalizing over the amount of transferred dies it increases to ~80% although there is much difference from die to die. In summary we can conclude that with each tier the die transfer yield decreased (100% for N=2, 93% for N=3 and 48% for N=4) and with it also the bond yield (~98% for N=2, ~90% for N=3 and ~80% for N=4). As mentioned previously, the lower transfer and bond yields are likely related to particles generated during insufficient back side cleaning of the dies after transfer.

#### IV. HYBRID BONDED N=3 STACK

Considering the good N=3 stacking results one such build was repeated using full loop dies with hybrid bond pads. The fabrication of these dies will be discussed elsewhere as it is out



**Figure 11. Cartoon of N:3 stack with hybrid bond pads and TSVs (left), Cross sectional SEM of a 5 μm pitch connection in the N=3 interface.**

of the scope of this work. In short, it involves an optimization of the dielectric surface, including hybrid bond pads, TSVs and finally the back side dielectrics with hybrid bond pads. Here, as a conclusion to this initial work, and as a demonstration of a more real life like application, only the cross section of such an N=3 die-stack will be discussed. Both front and back side hybrid bond pads consist of different pitch sizes ranging from 20 μm to 5 μm pitch. The collective die-to-wafer bonding step was identical to the flow discussed above (Fig. 1 and 2). After the final transfer, the N=3 stack was annealed up to 350°C to enable the Cu connections to form. Several such dies were submitted for cross sectional SEM (Fig 11) in order to visualize the N=3 connections. Both connectivity and die-to-die alignment are excellent in the shown stack.

#### V. CONCLUSIONS

Although a lot of work has been published in collective die-to-wafer bonding, truly little has been done on using this flow for multi-tier die stacking. Within this publication it is shown that the proposed imec collective-die-to-wafer bonding flow, including laser debonding with laser release layer and acoustic layer, can be extended to the multi-tier level. Although much optimization still needs to be done, mostly regarding die cleaning, several N=3 stacks were prepared with transfer yields up to 93% and bond yields up to 90%. Similar die-to-target wafer alignment results can be obtained as for the tier 1 level (Majority of the dies below 2 μm). Further extension to the N=4 level was less successful as the transfer yield decreased to 48% with much lower bond yield (~80%). Finally, an N=3 stack was built with hybrid bond pads and TSVs to evaluate the hybrid bond interface between die 1 and die 2 using cross sectional SEM, which shows excellent connectivity between the 2 dies for the 5 μm pitch.

#### ACKNOWLEDGEMENTS

The authors would like to thank Frank Lauterbach, Mike Soules, Hans Mathee and Stefan Lutter from SUSS MicroTec, Jakob Visker, Koen Smolders, David Huls, Lan Peng from imec for their support during the experiments. This work is carried within the frame of the imec 3DSystem Integration Industrial Affiliation Program and within a Joint Development Project between imec and SUSS MicroTec; and between imec and Brewer Science.

#### REFERENCES

- [1] P. Leduc et al., "First integration of Cu TSV using die-to-wafer direct bonding and planarization," 2009 IEEE International Conference on 3D System Integration, San Francisco, CA, 2009, pp. 1-5.J.
- [2] L. Sanchez et al., "Chip to wafer direct bonding technologies for high density 3D integration," 2012 IEEE 62nd Electronic Components and Technology Conference, San Diego, CA, 2012, pp. 1960-1964.
- [3] Teng Wang et al., "On the feasibility of die-to-wafer inorganic dielectric bonding," 2016 6th Electronic System-Integration

- Technology Conference (ESTC), Grenoble, 2016, pp. 1-5.
- [4] A. Phommahaxay et al., "Enabling Ultra-Thin Die to Wafer Hybrid Bonding for Future Heterogeneous Integrated Systems," 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 2019, pp. 607-613. doi: 10.1109/ECTC.2019.00097
- [5] S. Suhard et al., "Demonstration of a collective hybrid die-to-wafer integration using glass carrier," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 2064-2070
- [6] S. Suhard et al., "Demonstration of a collective hybrid die-to-wafer integration," 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2020, pp. 1315-1321
- [7] K. Kennes et al., "Acoustic modulation during laser debonding of collective hybrid bonded dies" 2021 IEEE 71th Electronic Components and Technology Conference (ECTC), 2126-2133
- [8] K. Kennes et al., "Carrier Systems for Collective Die-to-Wafer Bonding," 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 2058-2063
- [9] K. Kennes et al., "Introduction of a New Carrier System for Collective Die-to-Wafer Hybrid Bonding and Laser-Assisted Die Transfer" 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), 296-302
- [10] S. Suhard et al. "Integration of plasma dicing in the collective die to wafer hybrid bonding process. 2023 IEEE 25<sup>th</sup> Electronic Packaging and Technology Conference (EPTC) 548-553